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A METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT PACKAGE

ABSTRACT

A method of manufacturing an integrated circuit package such as a BGA package for use with an integrated circuit chip. The integrated circuit package has a substrate formed with a cavity that exposes a lower conductive level in the package so that connections between the integrated circuit chip and the lower conductive level may be formed to reduce the through holes formed in the substrate. As a result, additional signal line interconnections may be included in the substrate circuit package and/or the size of the integrated circuit chip may be decreased. Each of these may be implemented for enhanced electrical performance. The multiple wire bonding tiers in the substrate may also provide greater wire separation that eases wire bonding and subsequent encapsulation processes.